



Form PTO-1449 (modified)		Atty. Docket No. 2000.039000/TT3763	Serial No. 09/871,084
Office of Patents and Publications for Applicant's  INFORMATION DISCLOSURE STATEMENT  (Use several sheets if necessary)		Applicant Weber et al.	
		Filing Date: May 30, 2001	Group: 2131
U.S. Patent Documents <i>See Page 1</i>	Foreign Patent Documents <i>See Page 1</i>	Other Art <i>See Page 1</i>	

**U.S. Patent Documents**

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
	A1						
	A2						
	A3						
	A4						
	A5						

**Foreign Patent Documents**

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						
	B2						
	B3						
	B4						
	B5						

**Other Art (Including Author, Title, Date Pertinent Pages, Etc.)**

Exam. Init.	Ref. Des.	Citation
<i>Wt</i>	C1	Intel, "Low Pin Count (LPC) Interface Specification Revision 1.0," pp. 1-31 (09/29/97)
<i>Wt</i>	C2	Standard Microsystems Corporation, "100 Pin Enhanced Super I/O for LPC Bus with SMBus Controller for Commercial Application," Part No. LPC47B37x, pp. 1-254 (06/17/99)
<i>Wt</i>	C3	FIPS Pub 140-1 Federal Information Processing Standards Publication, "Security Requirements for Cryptographic Modules" (01/11/1994)
<i>Wt</i>	C4	Intel, "Communication and Networking Riser Specification," Revision 1.0 (02/07/2000)
<i>Wt</i>	C5	"Handbook of Applied Cryptography" CRC Press 1997 pp. 154 - 157, 160 - 161, 191 - 198, 203 - 212.

EXAMINER:

*Wt*

DATE CONSIDERED:

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